In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, lines 2 to 10 as follows:

--The invention is related to and claims priority under 35 USC 119(e)(1) from the following co-pending U.S. Provisional Patent Application serial No. 60/172,516 by Lu et al., entitled A Programmable Multi-standard MAC Architecture, and filed on Dec. 17, 1999; and serial No. 60/172,541 by Lu et al., entitled DSP Core/PHY Interface Specification, and filed on Dec. 17, 1999. In addition, the invention is related to the simultaneously filed co-pending U.S. Patent Application serial No. ~~(docket number TI-30141)~~ 09/737,722, entitled MAC/PHY Interface, by Lu et al. All of the aforementioned patent applications are hereby incorporated by reference:--

Rewrite the paragraph at page 10, lines 11 to 15 as follows:

--The Forward Pointer 430 is a 4 bit field which contains a pointer to the next queue descriptor in the same queue. There ~~maybe~~ may be some address limit on the start of a queue descriptor. When the pointer is 0, the current queue descriptor is the last one in the queue. When the last queue descriptor is processed, an event alert is raised for the queue.--

Rewrite the paragraph at page 25, lines 7 to 19 as follows:

--Referring now to Figure 7 there is shown an interface signal exchange between the MAC 705 portion and the PHY 710 portion of the HomePNA digital chip set 600 in accordance with an exemplary embodiment of the present invention. The transmit data bits ~~(TxD7-TxD0)~~ (TxD7-TxD0) are driven by the MAC 705. ~~(TxD7-TxD0)~~ (TxD7-TxD0) transition synchronously with respect to the Clk. For each period of the Clk when both the Transmit On (TxON) and

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Transmit Enable (TxEn) signals are asserted, ~~(TxD7-TxD0)~~ (TxD7-TxD0) are valid and available to the PHY 710. The ~~TxD7-TxD0~~ TxD7-TxD0 signals remain unchanged ~~until~~ while the TxEn signal is asserted. While TxON or TxEn is de-asserted, ~~(TxD7-TxD0)~~ (TxD7-TxD0) has no effect upon the PHY 710. TxD7 is the most significant bit (MSB) and ~~TxD0~~ TxD0 is the least significant bit (LSB). The TxD7-TxD0 bits are extended from MII interface bits TxD3-TxD0 into an eight bit data bus for the purpose of the data direct memory access (DMA) from the DSP.--

Rewrite the paragraph at page 26, lines 1 to 14 as follows:

--The TxON signal is used for two purposes: transmit frame and transmit backoff signal. This signal has been modified from a MII interface to accommodate the HomePNA backoff signals after collision. Regarding transmit frame, TxON indicates that the MAC 705 is presenting a frame on ~~(TxD7-TxD0)~~ (TxD7-TxD0) for transmission. It is asserted by the MAC 705 synchronously with the first byte of a Frame Control field of a HomePNA 2.0 frame and remains asserted while all the bytes being transmitted are presented to the PHY 710. When TxON is asserted, the PHY 710 uses the TxEn signal to indicate that ~~(TxD7-TxD0)~~ (TxD7-TxD0) are valid with a new data byte. For HomePNA systems, the PHY 710 transmits a frame prepended with PEAMBLE64 to the wire. PREAMBLE64 is a HomePNA PHY layer framing header known in the art. The PHY 710 continues to transmit until TxON is de-asserted. The PHY 710 ends transmission with EOF. Preferably, TxON is asserted for at least 92.5 μ s (TX_FRAME). Figure 8 shows the relative timing of the TxON signal in relation to a frame transmission with no collisions.--

Rewrite the paragraph at page 27, liens 3 to 6 as follows:

--A 1.0 Mode On (TxV1M1) assertion indicates that an HPNA 1.0 frame is being transmitted on ~~TxD7-TxD0~~ TxD7-TxD0 during TxON

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assertion. TxV1M1 remains asserted during the entire period of frame transmission. The TxV1M1 signal is a new signal on top of a MII interface.--

Rewrite the paragraph at page 27, lines 7 to 12 as follows:

--The reference clock (Clk) is a continuous clock locked, for example, at 32 MHz and is sourced by the PHY 710. The Clk provides the timing reference for the TxON, TxEn, and ~~TxD7-TxD0~~ TxD7-TxD0 signals for data transmission from the MAC 705 to the PHY 710. The Clk also provides the timing reference for the transfer of RxON, RxEn, and ~~RxD7-RxD0~~ RxD7-RxD0 signals for data transmission from the PHY 710 to the MAC 705.--

Rewrite the paragraph at page 27, line 13 to page 28, line 3 as follows:

--The receive bits ~~RxD7-RxD0~~ RxD7-RxD0 signals transition synchronously with respect to the Clk signal. ~~RxD7-RxD0~~ RxD7-RxD0 are driven by the PHY 710. For each Clk period in which both RxON and RxEn are asserted, ~~RxD7-RxD0~~ RxD7-RxD0 provides eight valid bits of decoded data from the PHY 710 to the MAC 705. ~~RxD7-RxD0~~ RxD7-RxD0 remain valid ~~until~~ while a Receive Enable (RxEn) signal is asserted. While Receive Data On (RxON) or RxEn is de-asserted, ~~RxD7-RxD0~~ RxD7-RxD0 are invalid. RxD7 is the most significant bit (MSB) and ~~RxD0~~ RxD0 is the least significant bit (LSB). The RxD7-RxD0 bits are extended from MII interface bits RxD3-RxD0 into an eight bit data bus for the purpose of the data direct memory access (DMA) to the DSP.--

Rewrite the paragraph at page 28, lines 4 to 15 as follows:

--The RxON signal is used for two purposes: receive Frame and receive backoff signal. The use of this signal has been modified from a MII interface to accommodate the HomePNA backoff signals

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after collision. For frame receiving, the RxON is provided by the PHY 710 to indicate that the PHY 710 has valid decoded data bits on ~~RxD7-RxD0~~ RxD7-RxD0. The data on the ~~RxD7-RxD0~~ RxD7-RxD0 is synchronous to the Clk and RxON transitions synchronously with respect to the Clk. Further, RxON remains asserted continuously from the first decoded bit of a frame (without preamble) through the final bit of the frame (without EOF) and is negated prior to the first Clk cycle that follows the final nibble. Upon RxON assertion, the PHY 710 starts sending the RxEn signal which indicates that a valid data byte is present on ~~RxD7-RxD0~~ RxD7-RxD0. Figure 9 shows the relative timing of RxON during a frame reception.--

Rewrite the paragraph at page 29, lines 3 to 12 as follows:

--The TxEn signal is sourced by the PHY 710 to signal the MAC 705 to place new data on ~~TxD7-TxD0~~ TxD7-TxD0. Once TxON is asserted, the PHY 710 provides TxEn pulses (one pulse is 1/32 MHz cycle wide) to indicate that the MAC 705 can place new valid data on TxD7-TxDO. The average rate of the TxEn pulses is the transmission data rate in bytes, which is about 4 MHz for a 32 Mbps data rate. This signal provides for transmitting data between the MAC 705 and the PHY 710 at a variable rate which matches the PHY's data rate. Upon de-assertion of the TxON signal, the PHY 710 stops supplying TxEn pulses. The TxEn signal timing during a data transmission from the MAC 705 to the PHY 710 is shown in Figure 8.--

Rewrite the paragraph at page 29, line 13 to page 30, line 2 as follows:

--Referring back to Figure 7, the RxEn signal is sourced by the PHY 710 to signal the MAC 705 that new data has been placed on ~~RxD7-RxD0~~ RxD7-RxD0 signal lines. The RxEn signal is only valid

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while the RxON signal is asserted. The average rate of the RxEn signal pulses will be the transmission data rate in bytes, which is around 4 MHz for a 32 Mbps data rate. This signal provides for transmitting data between MAC 705 and PHY 710 at a variable rate to match the PHY's data rate. RxEn signal operation during data transmission from the PHY 710 to the MAC 705 is shown in Figure 9.--

Rewrite the paragraph at page 31, lines 9 to 12 as follows:

--A Receive HPNA 1.0 Frame (RxVIMI) signal is provided by the PHY 705 to indicate a detection of a HPNA 1.0 frame. This signal is asserted during the entire period of RxON signal assertion if the data on ~~RxD7-RxD0~~ RxD7-RxD0 is a HPNA 1.0 frame.--

Rewrite the paragraph at page 38, lines 1 to 16 as follows:

--Exemplary DSP/PHY interface signals used for sample data transfer from the PHY 620 to the DSP module 640 include: SampOn, SampEn, SampD15-SampD0. The SampON signal is used to transmit a block of sample data from the PHY 620 to the DSP module 640. The SampON signal is provided by the PHY 620 to indicate that the PHY 620 has valid sample data bits on SampD15-SampD0. SampON remains asserted continuously from the first word of a block of sample data through the final word of the block of sample data. Upon SampON assertion, the PHY 620 starts sending the SampEn signal which indicates that a valid sample word is present on ~~SampD15-SampD0~~ SampD15-SampD0. The SampEn signal is sourced by the PHY 620 to signal the DSP module 640 that new sample data has been placed on ~~SampD15-SampD0~~ SampD15-SampD0 signal lines. The average rate of the SampEn signal pulses is the transmission sample rate, which can be, for example, around 8 MHz. The ~~SampD15-SampD0~~ SampD15-SampD0 signals transition synchronously with the SampEn signal pulses. ~~SampD15-SampD0~~ SampD15-SampD0 are driven by the PHY 620. For each

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period of SampEn asserted, ~~SampD15-SampD0~~ SampD15-SampD0 provides sixteen valid sample data bits from the PHY 620 to the DSP module 640.--

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